EQ/2/0 14/2/03

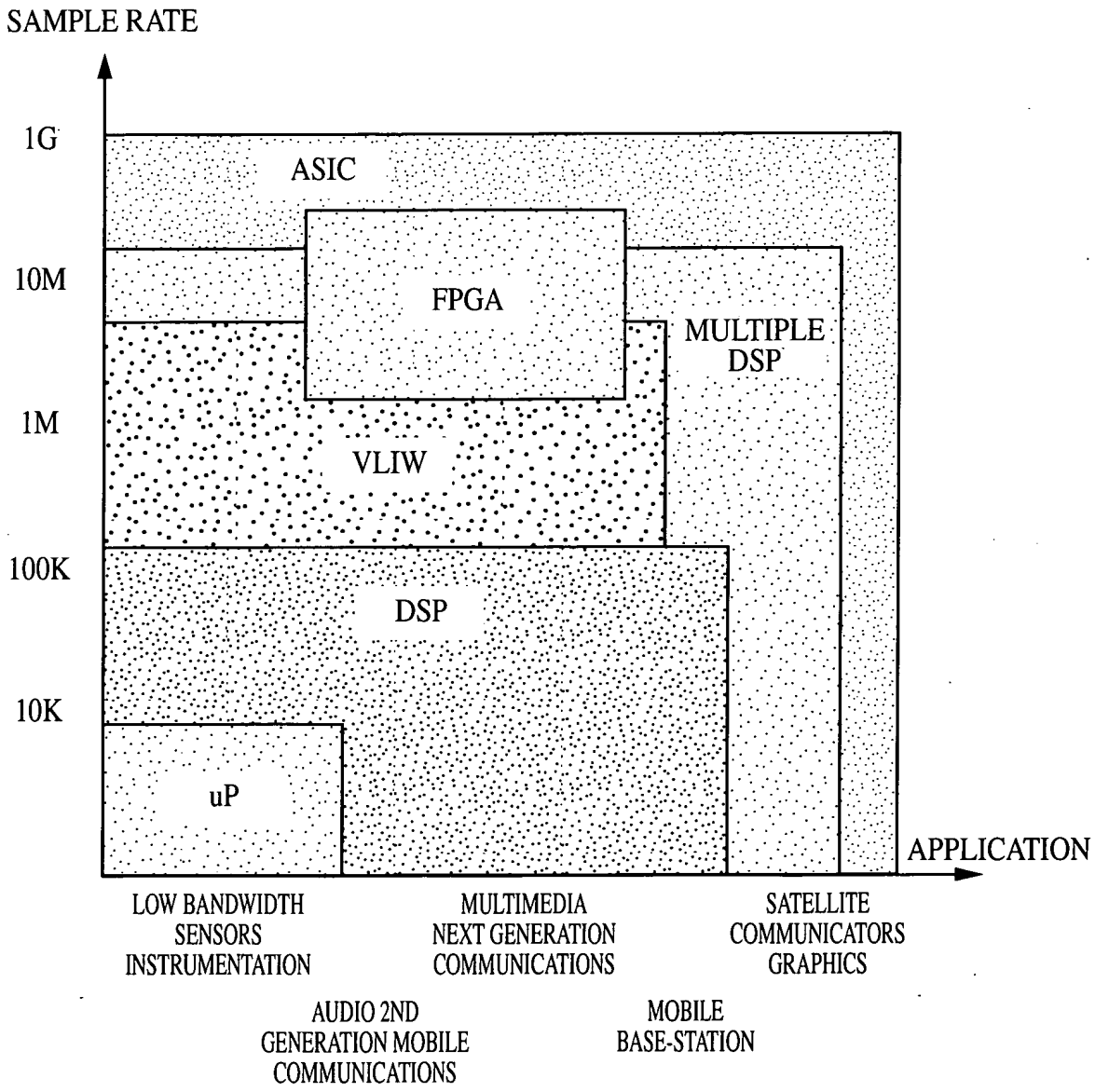


FIG. 1

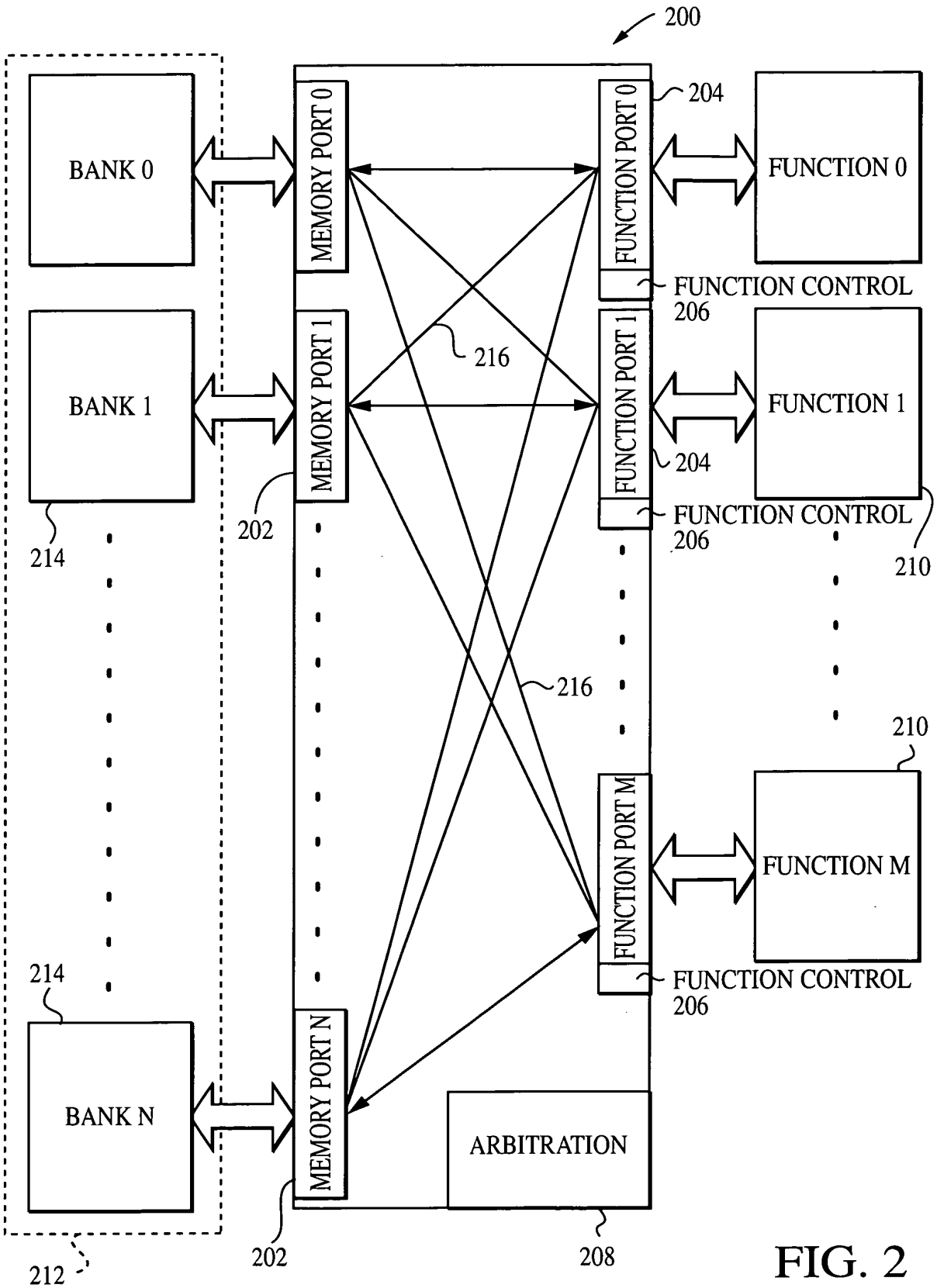

200
BANK 0
BANK 1
BANK N
MEMORY PORT 0
MEMORY PORT 1
MEMORY PORT N
FUNCTION PORT 0
FUNCTION PORT 1
FUNCTION PORT M
FUNCTION 0
FUNCTION 1
FUNCTION M
FUNCTION CONTROL
206
204
216
214
202
210
ARBITRATION
208
212

FIG. 2

T0270 Th2T0860

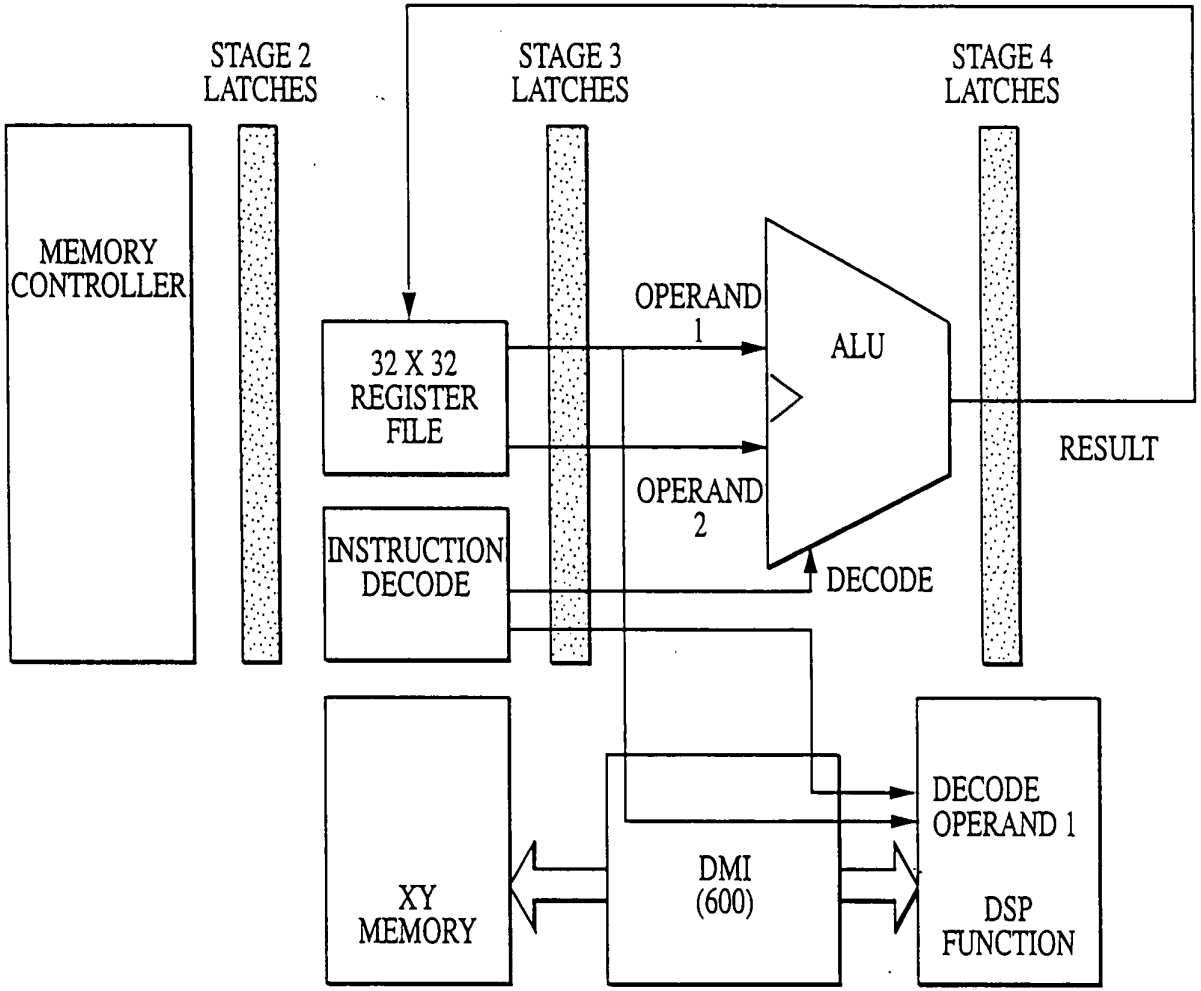


FIG. 2a

09/827,203 - 04/25/2001

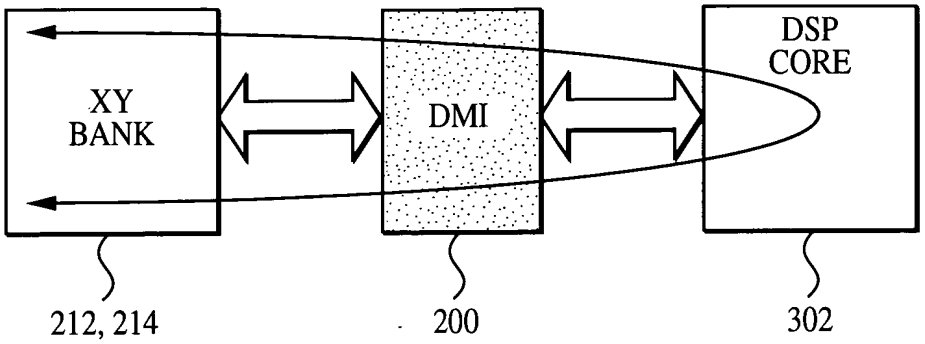


FIG. 3

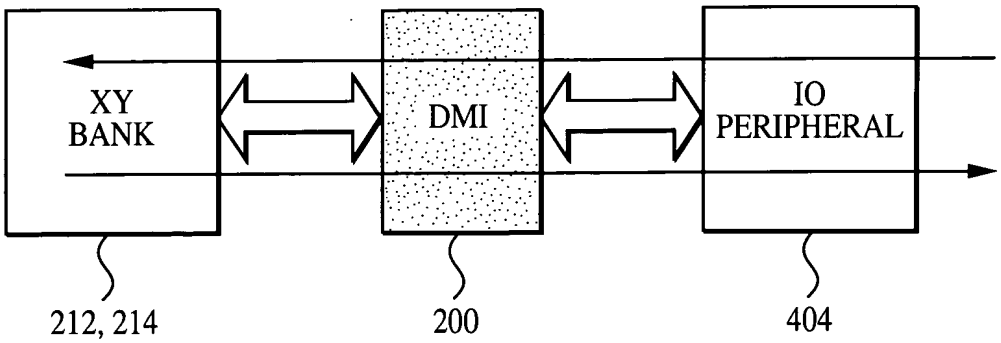


FIG. 5

09814241 .072704

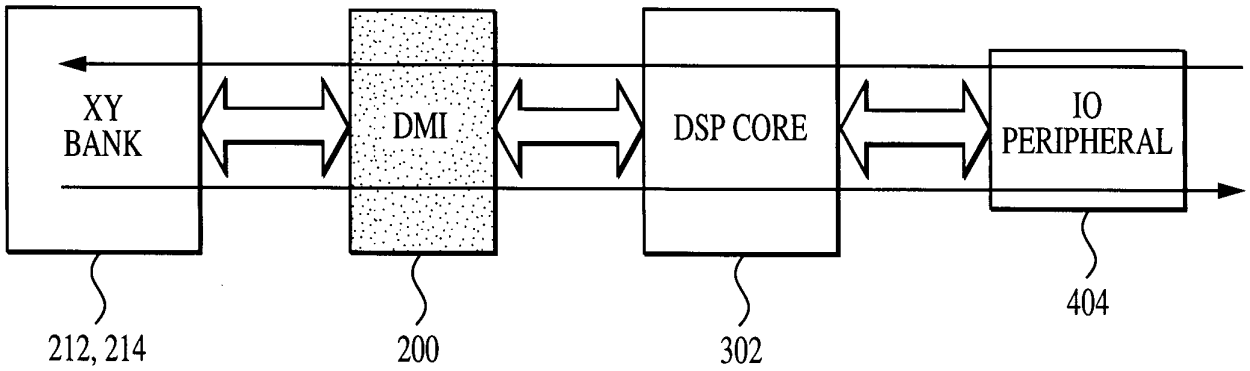


FIG. 4

T07270 Th2T0860

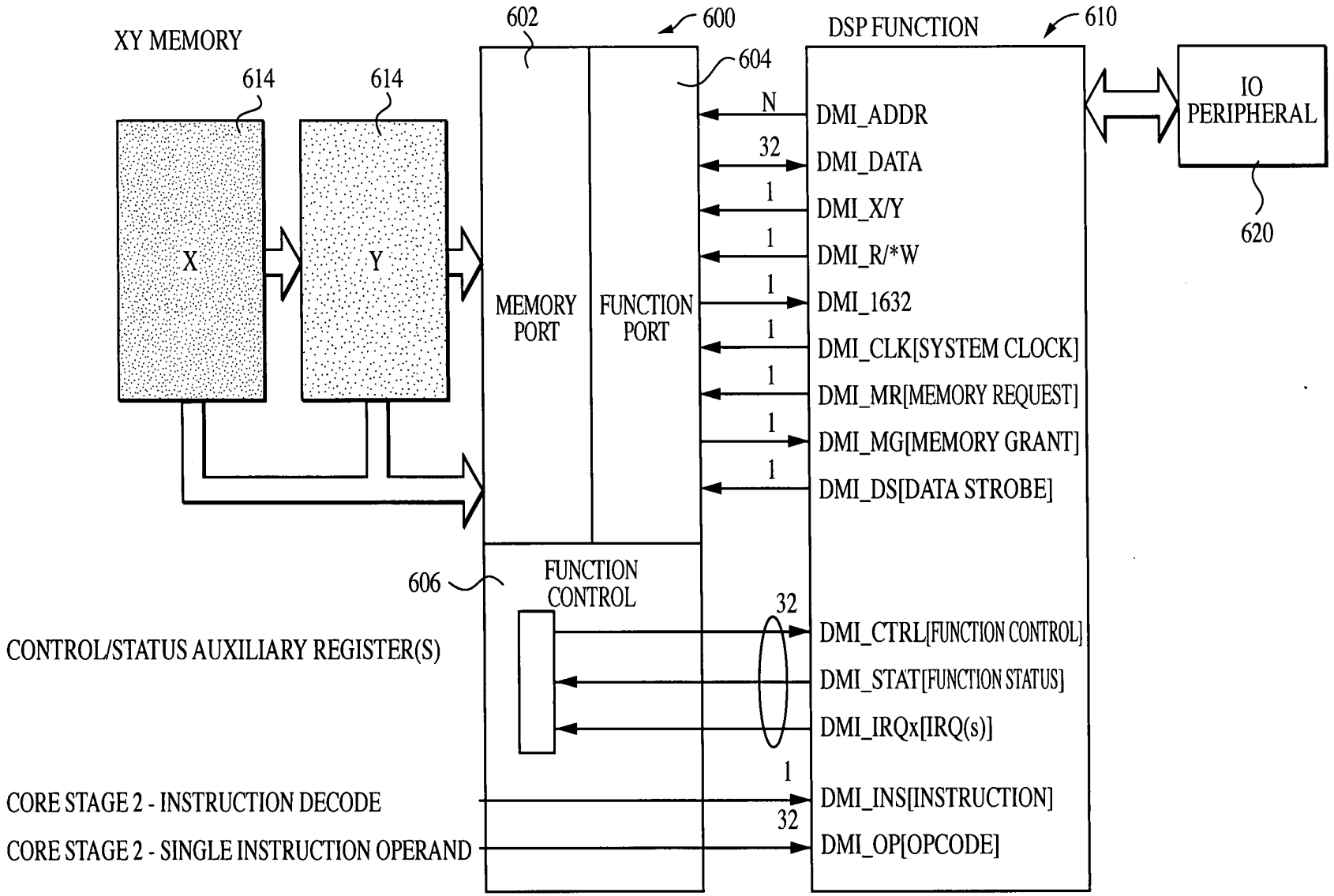
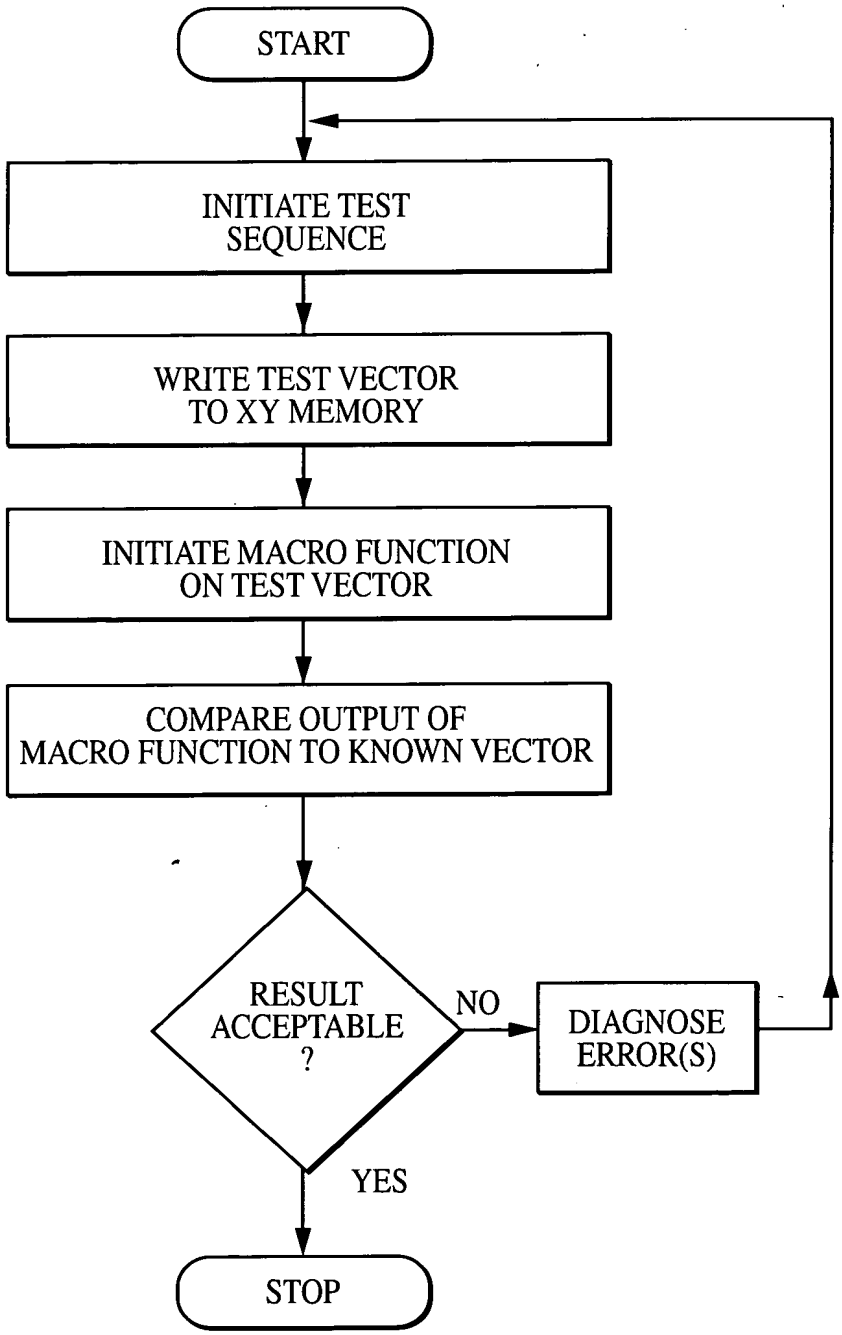


FIG. 6

FIG. 6a


START
INITIATE TEST SEQUENCE
WRITE TEST VECTOR TO XY MEMORY
INITIATE MACRO FUNCTION ON TEST VECTOR
COMPARE OUTPUT OF MACRO FUNCTION TO KNOWN VECTOR
RESULT ACCEPTABLE ?
NO
DIAGNOSE ERROR(S)
YES
STOP

T0270 Th2T0360

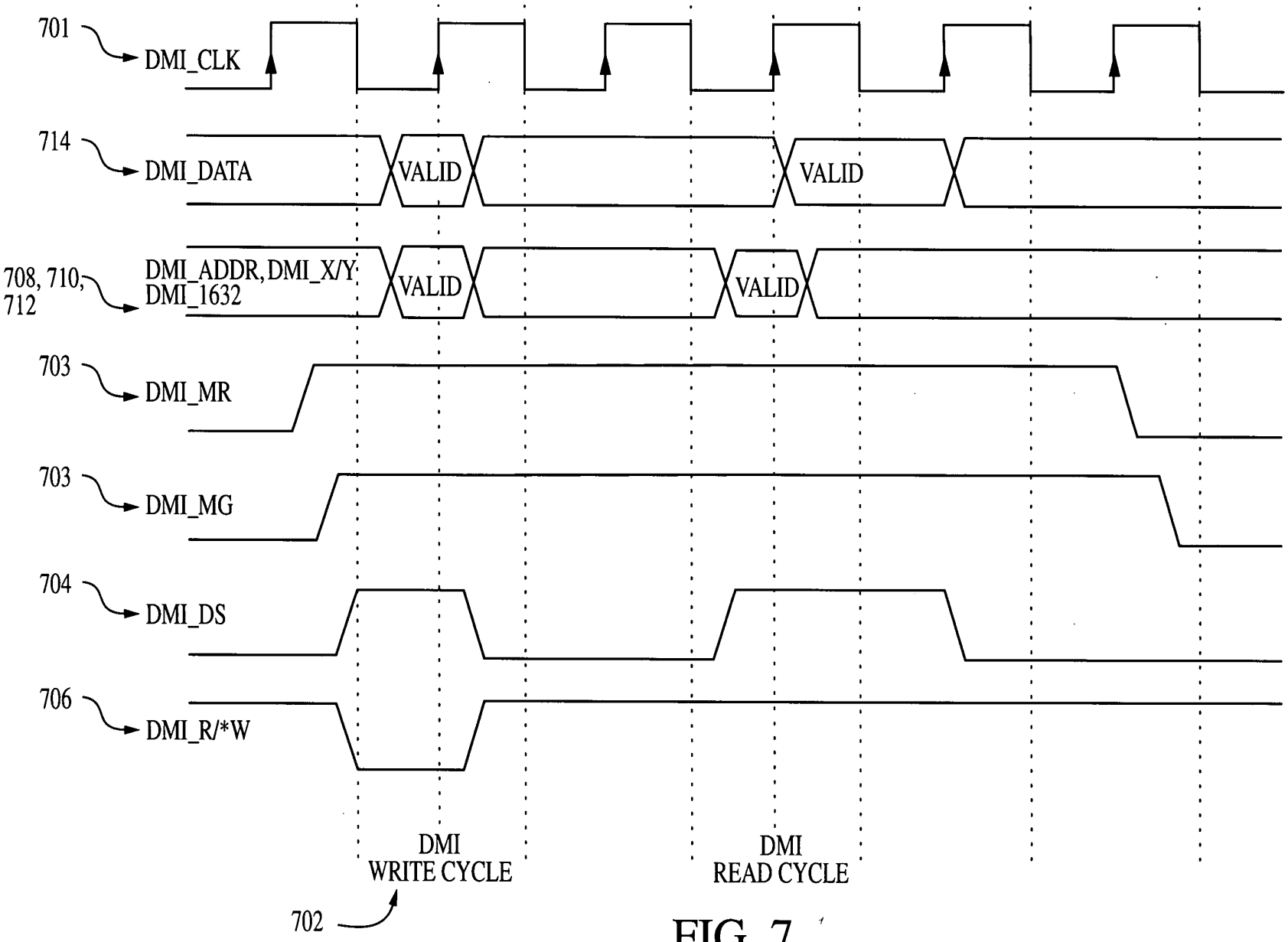


FIG. 7

T07270 Th2T0860

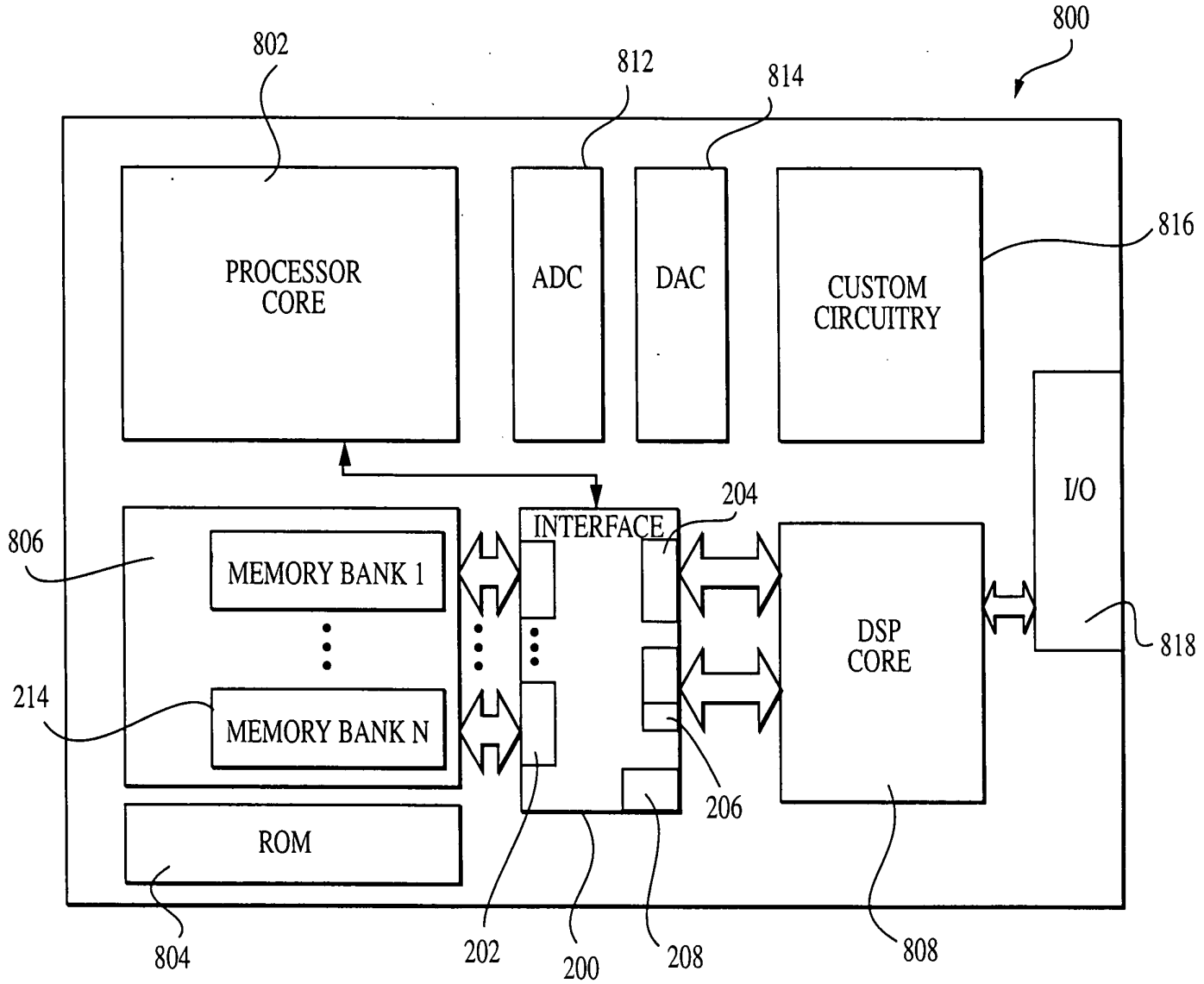


FIG. 8

T0270" Th2T0860

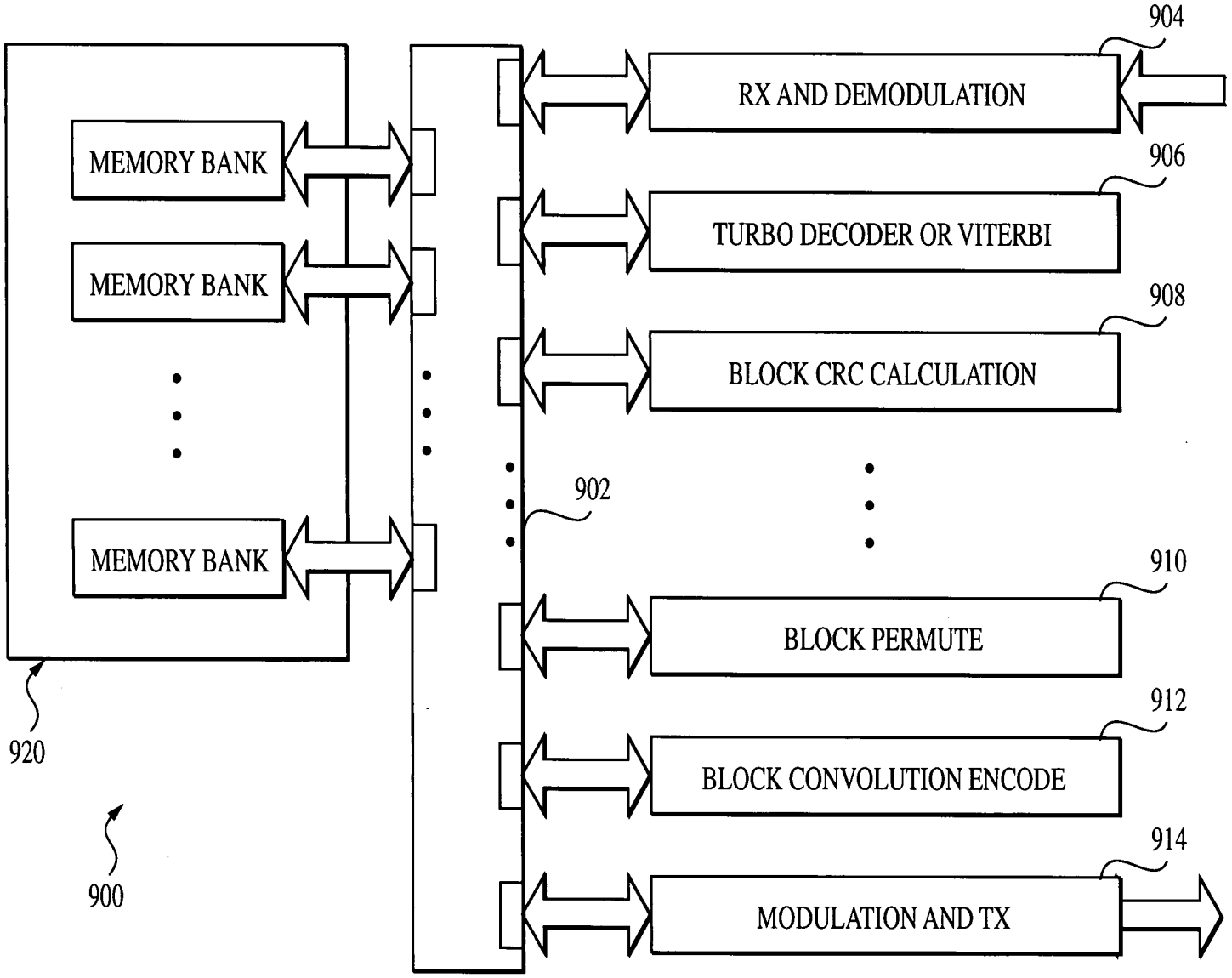


FIG. 9

	Data Block 0	Data Block 1	Data Block 2	Data Block 3	Data Block 4	...
Bank 0	Function 0	Function 1	Function 2	Function 3	Function 0	
Bank 1	-	Function 0	Function 1	Function 2	Function 3	
Bank 2	-	-	Function 0	Function 1	Function 2	
Bank 3	-	-	-	Function 0	Function 1	

FIG. 9a

FIG. 10

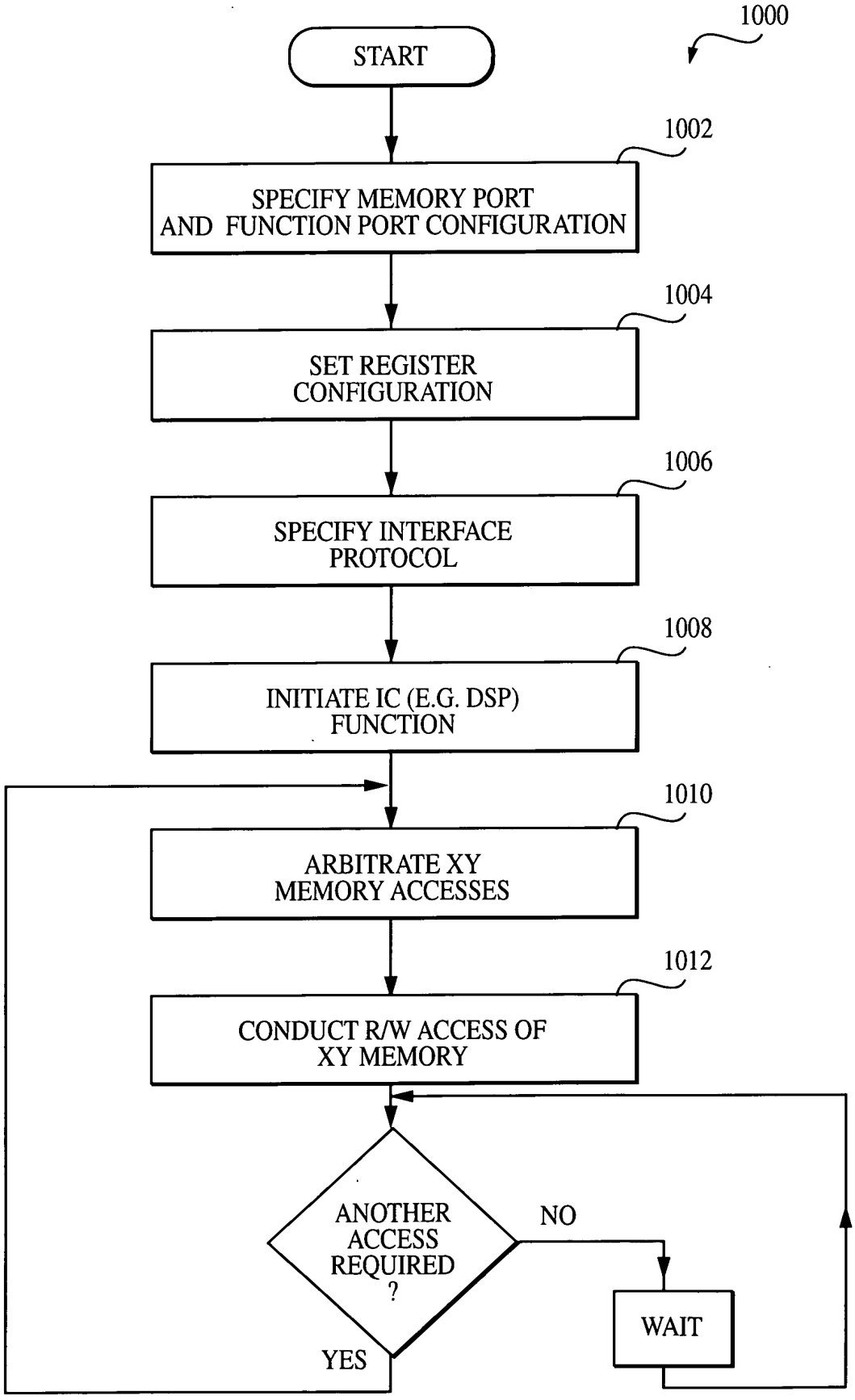

1000
START
1002
SPECIFY MEMORY PORT AND FUNCTION PORT CONFIGURATION
1004
SET REGISTER CONFIGURATION
1006
SPECIFY INTERFACE PROTOCOL
1008
INITIATE IC (E.G. DSP) FUNCTION
1010
ARBITRATE XY MEMORY ACCESSES
1012
CONDUCT R/W ACCESS OF XY MEMORY
ANOTHER ACCESS REQUIRED ?
NO
YES
WAIT

FIG. 11

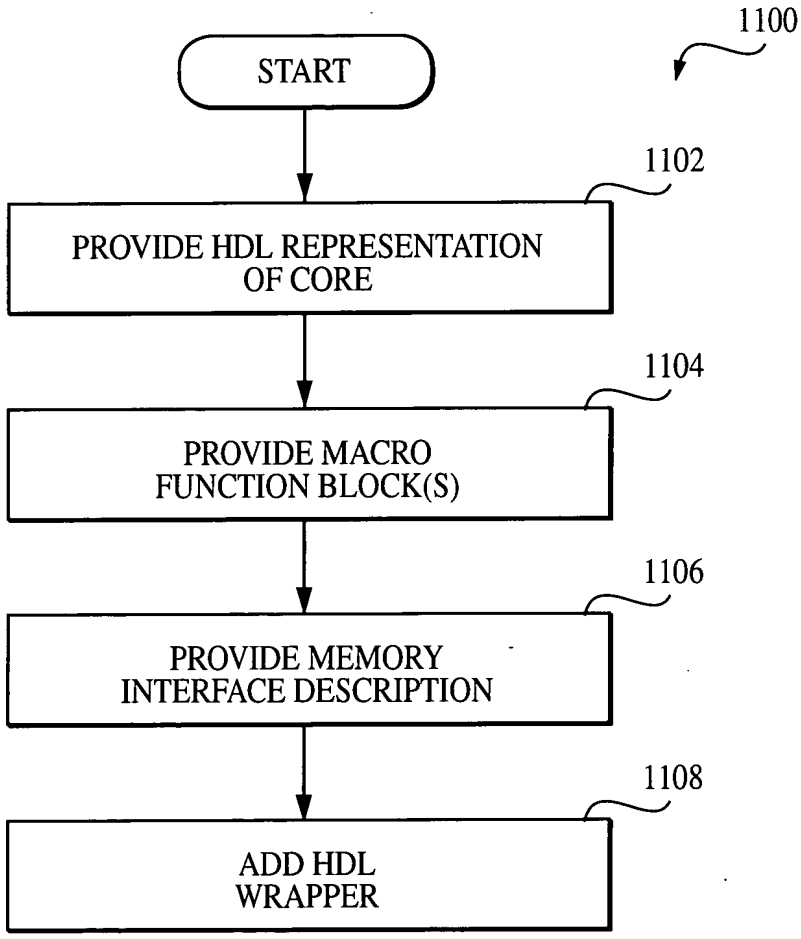

1100
START
1102
PROVIDE HDL REPRESENTATION OF CORE
1104
PROVIDE MACRO FUNCTION BLOCK(S)
1106
PROVIDE MEMORY INTERFACE DESCRIPTION
1108
ADD HDL WRAPPER

FIG. 11a

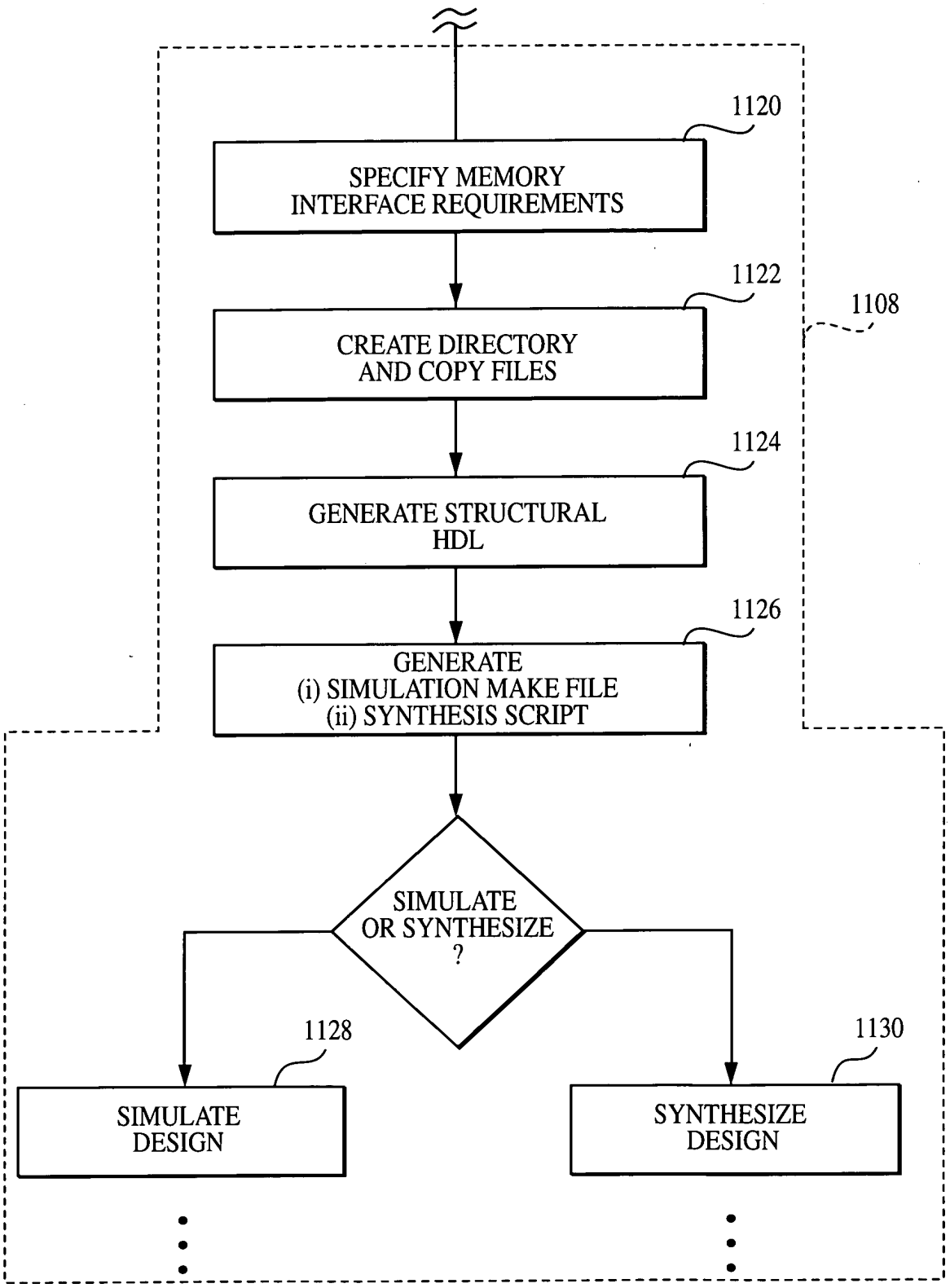
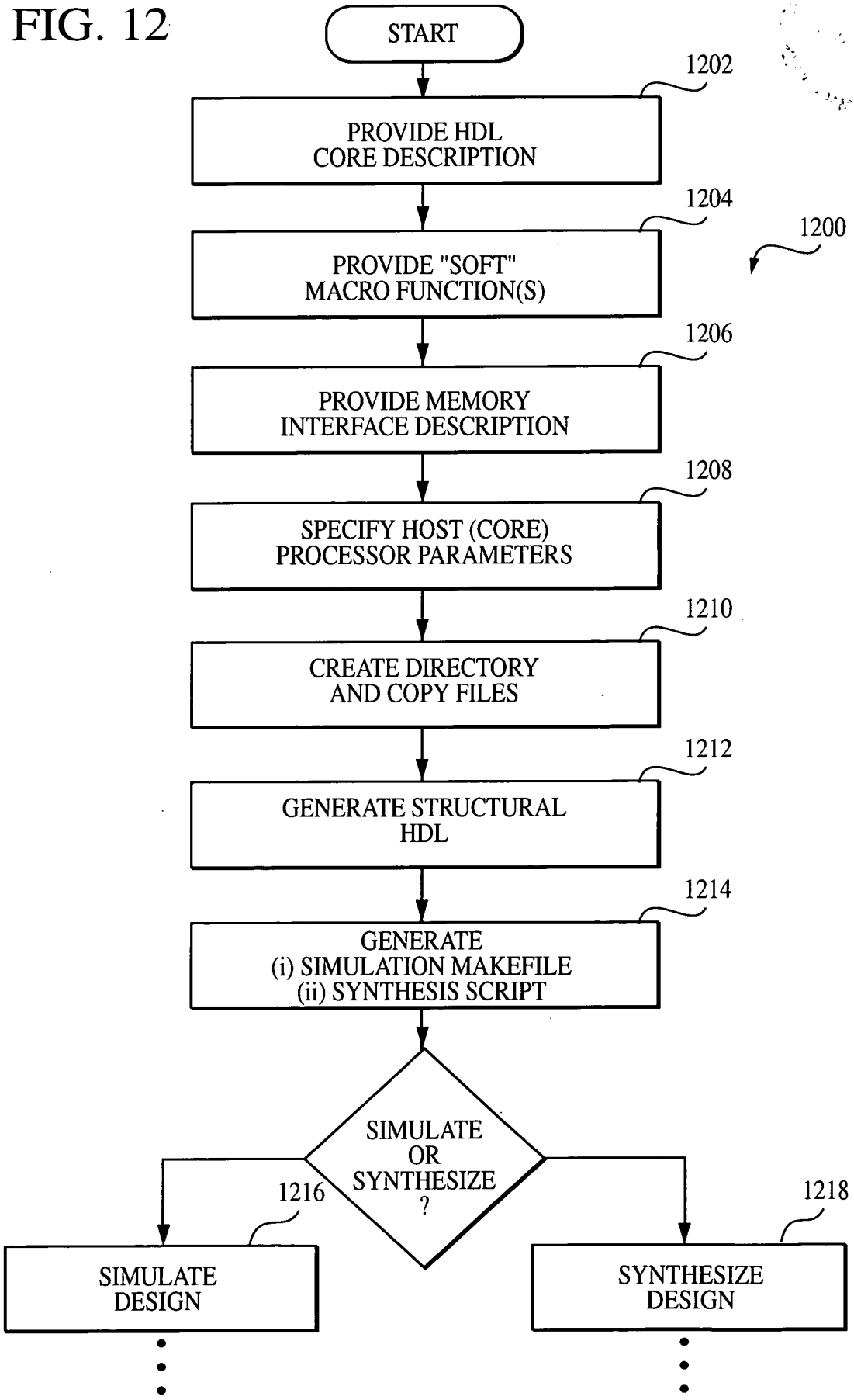

1120
SPECIFY MEMORY INTERFACE REQUIREMENTS
1122
CREATE DIRECTORY AND COPY FILES
1108
1124
GENERATE STRUCTURAL HDL
1126
GENERATE
(i) SIMULATION MAKE FILE
(ii) SYNTHESIS SCRIPT
SIMULATE OR SYNTHESIZE ?
1128
SIMULATE DESIGN
1130
SYNTHESIZE DESIGN

FIG. 12


START
1202
PROVIDE HDL CORE DESCRIPTION
1204
PROVIDE "SOFT" MACRO FUNCTION(S)
1200
1206
PROVIDE MEMORY INTERFACE DESCRIPTION
1208
SPECIFY HOST (CORE) PROCESSOR PARAMETERS
1210
CREATE DIRECTORY AND COPY FILES
1212
GENERATE STRUCTURAL HDL
1214
GENERATE (i) SIMULATION MAKEFILE (ii) SYNTHESIS SCRIPT
SIMULATE OR SYNTHESIZE ?
1216
SIMULATE DESIGN
1218
SYNTHESIZE DESIGN